IN THE CLAIMS:

All of the claims that remain pending and under consideration in the above-referenced application are presented, pursuant to 37 C.F.R. §§ 1.121(c)(1)(i) and 1.121(c)(3), in clean form below. Claims 1 and 15 have been amended. Please enter these claims as amended. Also attached is a marked-up version of the claims, as amended herein, pursuant to 37 C.F.R. § 1.121(c)(1)(ii).

Please amend the claims as follows:

1. (Four Times Amended) A semiconductor die assembly comprising:

a semiconductor substrate having a first surface and a second surface, wherein said semiconductor substrate includes at least one opening defined therethrough between said semiconductor substrate first surface and said semiconductor substrate second surface;

at least one semiconductor die having an active surface with at least one electrical connection area disposed on said semiconductor die active surface, said at least one semiconductor die oriented having said at least one electrical connection area substantially aligned with said at least one semiconductor substrate opening; and

at least one adhesive tape interposed between and attaching said semiconductor die active surface and said semiconductor substrate first surface, wherein a width of said at least one adhesive tape extends at least proximate an edge of said at least one semiconductor die to an edge of said at least one semiconductor substrate opening.

2. (Previously Amended) The semiconductor die assembly of claim 1, wherein said width of said at least one adhesive tape extends beyond said edge of said at least one semiconductor substrate opening a distance into said at least one semiconductor substrate opening to provide a detectable surface within said at least one semiconductor substrate opening.

3. (Previously Amended) The semiconductor die assembly of claim 1, wherein said width of said at least one adhesive tape extends beyond said edge of said at least one semiconductor die

a distance on said semiconductor substrate first surface to provide a detectable adhesive tape surface on said semiconductor substrate first surface.

4. The semiconductor die assembly of claim 1, further including at least one electrical connection extending between said at least one electrical connection area and at least one trace on said semiconductor substrate second surface.

5. The semiconductor die assembly of claim 4, wherein said at least one electrical connection comprises a bond wire.

6. The semiconductor die assembly of claim 4, wherein said at least one electrical connection comprises a TAB connection.

7. The semiconductor die assembly of claim 4, further including a glob top material disposed within said at least one semiconductor substrate opening encasing said at least one electrical connection.

8. The semiconductor die assembly of claim 7, further including an encapsulant material encasing said at least one semiconductor die and said glob top material.

9. The semiconductor die assembly of claim 1, wherein said at least one adhesive tape comprises a planar carrier film including a first surface having a first adhesive disposed thereon and a second surface having a second adhesive disposed thereon.

10. The semiconductor die assembly of claim 9, wherein a composition of said first adhesive differs from a composition of said second adhesive.

11. The semiconductor die assembly of claim 1, further comprising at least one fillet located proximate said at least one adhesive tape and said edge of said at least one semiconductor die.

12. The semiconductor die assembly of claim 1, further comprising at least one fillet located proximate said at least one adhesive tape and said edge of said at least one semiconductor substrate opening.

13. The semiconductor die assembly of claim 1, further comprising at least one fillet located proximate said at least one adhesive tape and said active surface of said at least one semiconductor die.

14. The semiconductor die assembly of claim 1, further comprising at least one fillet located proximate said at least one adhesive tape and said semiconductor substrate first surface.

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15. (Three Times Amended) A computer comprising:

at least one semiconductor die assembly, said semiconductor die assembly comprising:

a semiconductor substrate having a first surface and a second surface, wherein said semiconductor substrate includes at least one opening defined therethrough between said semiconductor substrate first surface and said semiconductor substrate second surface;

at least one semiconductor die having an active surface with at least one electrical connection area disposed on said semiconductor die active surface, said at least one semiconductor die oriented having said at least one electrical connection area substantially aligned with said at least one semiconductor substrate opening; and

at least one adhesive tape interposed between and attaching said semiconductor die active surface and said semiconductor substrate first surface, wherein a width of said at least one adhesive

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tape extends at least proximate an edge of said at least one semiconductor die to an edge of said at least one semiconductor substrate opening.